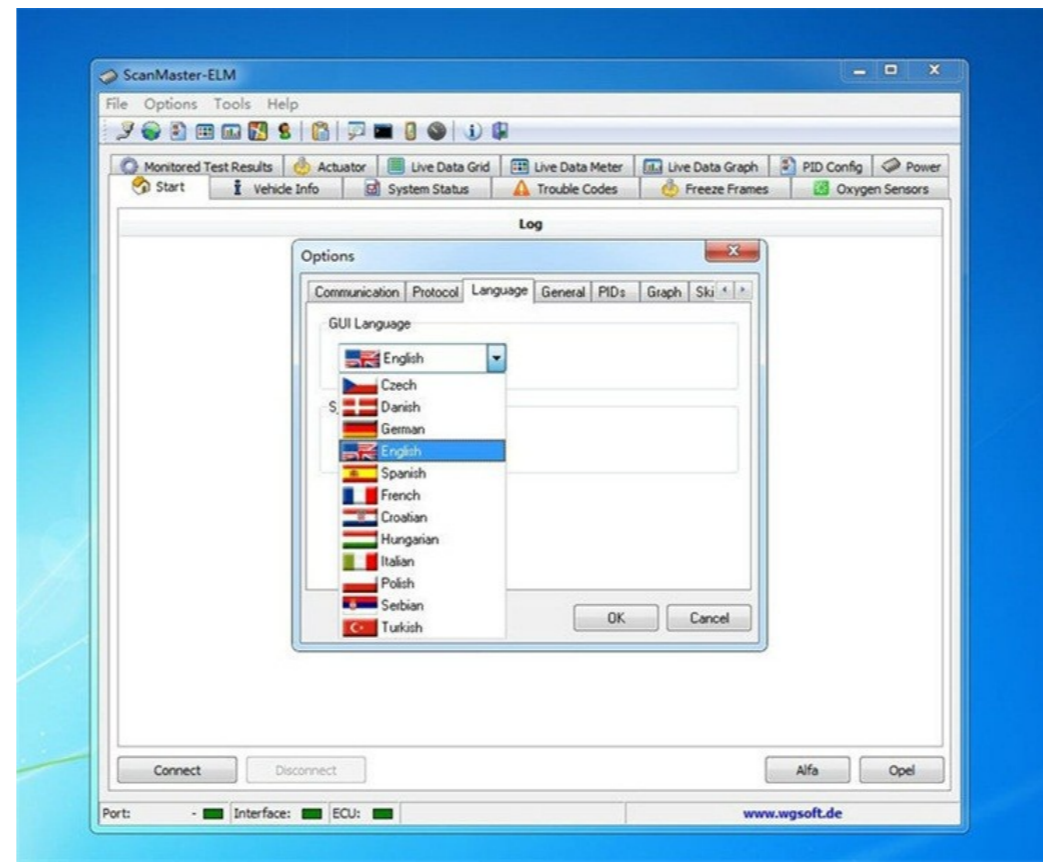


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/ u32 vid0_fp_type; / Vertical fpd related */ u32 vid0_dtd; /* Frame and field rate */ u32 vid0_dfl_dtd; /* Default DP clock/hsync/pixel clock */ u32 vid0_dfl_fpd; /* Default HPD to VPD */ u32 vid0_col_start; /* First pixel on the left side of the * display, in pixels */ u32 vid0_col_end; /* Last pixel on the right side of the u32 vid0_pixel_start; /* First pixel on the display, in * pixels */ u32 vid0_pixel_end; /* Last pixel on the display, in pixels */ u32 vid0_xres; /* Horizontal resolution, in pixels */ u32 vid0_yres; /* Vertical resolution, in pixels */ u32 vid0_bpp; /* Bits per pixel */ u32 vid0_fmt; /* Pixel format */ u32 vid0_link_en; /* VPD-FPD link enable */ u32 vid0_link_sta; /* VPD-FPD link status */ u32 vid0_dual_link; /* VPD-FPD dual link support */ u32 vid0_lfp_pre_mode; /* VPD-FPD LFP pre enable */ u32 vid0_lfp_post_mode; /* VPD-FPD LFP post enable */ u32 vid0_dual_pre_mode; /* VPD-FPD dual pre enable */ u32 vid0_dual_post_mode; /* VPD-FPD dual post enable */ u32 vid0_link_bw; /* VPD-FPD link bandwidth */ u32 vid0_mpll_cfg0; /* Main PLL config 0 */ 82157476af

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